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## Document Listing

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| US006340629 | 6 | 1 - 6 |
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thermal $O_3$/TEOS USG film used in a conventional process) with low compressive stress capped with a PECVD USG capping layer to form a conformal, thin composite insulating layer suitable for use as an IMD layer in certain applications. All the experiments were performed in a lamp-heated Precision **5000** DCVD chamber (outfitted for 200-mm wafers) manufactured by Applied Materials, Inc. A $C_2F_6$—$NF_3$ two-step plasma clean was used after every deposition. The primary process recipe used in the experiments was as follows. For the discussion below, it is noted that flow rates of TEFS and TEOS are flow rates of vaporized TEFS with helium carrier gas and TEOS with helium carrier gas, respectively.

The FSG films were deposited at a temperature of 400° C. and at a pressure of 450 torr. Spacing between the susceptor and manifold was 230 mil. The flow rate of TEFS was 2400 sccm, and the flow rate of TEOS was 5000 sccm. Oxygen in the form of $O_3$ is introduced at a flow rate of 5000 sccm. The ozone mixture contained greater than 13 wt % oxygen. The FSG films deposited were 1 $\mu$m thick. Thirteen other processes were used by varying the deposition pressure, susceptor temperature and gas flow while keeping the other parameters the same as that in the above primary recipe.

FSG films deposited using these fourteen processes were evaluated by measuring the thickness, uniformity, stress and F concentration. Film thickness and uniformity were measured with a Prometrix™ SM300 film gauge (using 49 points, with 3-mm edge exclusion, 1 standard deviation). Film stress was measured with a Flexus™ 2300 stress gauge. Fluorine concentration was obtained by Fourier transform infrared (FTIR) spectroscopy.

The deposition rate of each process was calculated from the FSG film thickness after 2 minutes of deposition. FSG films with thickness of 1 $\mu$m capped with a 1000 Å PETEOS film were deposited to examine stress, FTIR and wet etch rate ratio. Because the water absorption of FSG film was expected to be very high, the 1000 Å thick PETEOS film was used as a cap layer, in this embodiment. The PETEOS film is a USG capping layer that is stable and does not readily absorb moisture. Thus, the USG capping layer provides a hydrophobic surface on top of the FSG layer that prevents moisture present in the ambient from being absorbed into the FSG film. Furthermore, the USG capping layer is a relatively dense film that impedes fluorine evolution.

In the experiments, the USG capping films were deposited onto the FSG films at a temperature of 400° C., a high RF power of 700 Watts, and at a pressure of 8.2 torr. Spacing between the susceptor and manifold was 230 mil. The flow rate of TEOS was 800 sccm. Oxygen in the form of $O_2$ is introduced at a flow rate of 600 sccm. The oxygen mixture contained greater than 13 wt % oxygen. The USG films deposited were 1000 Å thick.

FIGS. 3(*a*)–3(*c*) are graphs illustrating the effect on the FSG film by varying deposition pressure. The effect of varying the deposition pressure on the FSG film was studied by depositing FSG films using the primary recipe having pressure of 450 torr, and FSG films using the primary recipe but at varying pressures of 70, 200, and 600 torr. The relation between deposition rate and deposition pressure is shown in FIG. 3(*a*). The deposition rate had the highest value (4256 Å/min) at a pressure of 200 torr, and dropped at higher and lower pressures (e.g., about 3500 Å/min at 450 torr). Each capped FSG film was found to have low compressive stress. Stress as a function of time was measured to test the stability of the films. The capped FSG films were demonstrated to be stable films, as shown in FIG. 3(*b*) which illustrates that stress did not vary significantly over time for films that were deposited at lower pressures (about $-2.4\times10^9$ dynes/cm$^2$ at 70 torr, about $-1.9\times10^9$ dynes/cm$^2$ at 200 torr, about $-2.5\times10^8$ dynes/cm$^2$ at 450 torr). The F concentration was obtained from the FTIR spectrum by integrating the area under Si—F and Si—O peak. It was found that the F concentration, as shown in FIG. 3(*c*), increased as the deposition pressure increased for pressures lower than 450 torr. F concentration remained fairly constant at about 2.25 wt % for the capped FSG films deposited at pressures of 450 and 600 torr. The above experiments demonstrate that 1 $\mu$m thick FSG films exhibiting low compressive stress may be useful as IMD layers and may be formed at good deposition rates. The present FSG films with film properties suitable for IMD applications and having film thickness of about 1 $\mu$m advantageously have a minimized thickness compared to composite thermal $O_3$/TEOS capped USG films.

Next, the effect of varying the deposition temperature was investigated. Films were deposited with the primary recipe having susceptor temperature of 400° C., and with the primary recipe at different susceptor temperatures of 350° C. and 450° C. The deposition rates obtained for films deposited at these temperatures are listed in Table 1.

TABLE 1

| Temperature (° C.) | Deposition Rate (Å/min) |
|---|---|
| 350 | 2377 |
| 400 | 3453 |
| 450 | 2540 |

As seen in Table 1, the deposition rate was highest for the FSG film deposited at a temperature of 400° C., with lower deposition rates for films deposited at 350° C. and at 450° C. The F concentration of the FSG films having the higher deposition rates was measured to be about 2.26 wt % for the film deposited at 400° C. and about 1.67 wt % for the film deposited at 450° C. Thus, temperatures of approximately 400° C. appear to be the optimum temperature, to achieve a high deposition rate with higher F incorporation into the film. The deposition rate is desirably at least about 2300 Å/min, and preferably at least about 3000 Å/min. Advantageously it is at least about 3400 Å/min, and more preferably at least about 4000 Å/min. In a preferred embodiment, it is at least about 4500 Å/min. As shown below, the invention can provide such high deposition rates combined with good film properties.

FIGS. 4(*a*)–4(*c*) are graphs illustrating the effects on the FSG films by varying TEOS flow rates. The effects of varying flow rates for the TEOS were investigated by depositing capped FSG films using the primary recipe having TEOS at a flow rate of 5000 sccm, and films using the primary recipe but with varying TEOS flow rates of 3000 and 6000 sccm. FIG. 4(a) is a graph illustrating deposition rate as a function of TEOS flow. No film was deposited when the TEOS flow was set to 1000 sccm, and the deposition rate increased as TEOS flow increased, as seen in FIG. 4(*a*). FIG. 4(*b*) illustrates stress-time curves of films deposited at different TEOS flow rates, and shows that the stress of each of the three films changed with time. As seen in FIG. 4(*b*), FSG films were formed that had low compressive stress ranging between about as low as $-1.5\times10^8$ to $-2.7\times10^8$ dynes/cm$^2$. As discussed earlier, it is desirable to produce a film having stress of less than $-5\times10^8$ dynes/cm$^2$, and preferably less than $-4\times10^8$ dynes/cm$^2$. As seen in FIG. 4(*c*), the F concentration in the films decreased as the TEOS flow

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| Total (1) | 24 | 24 | 0 |

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(12) **United States Patent**
**Kwan et al.**

(10) **Patent No.: US 6,335,288 B1**
(45) **Date of Patent: Jan. 1, 2002**

(54) **GAS CHEMISTRY CYCLING TO ACHIEVE HIGH-ASPECT RATIO GAPFILL WITH HDP-CVD**

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(73) Assignee: **Applied Materials, Inc.**, Santa Clara, CA (US)

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(52) **U.S. Cl.** ..... **438/694**; 438/697; 438/784; 438/787; 438/788; 438/911; 427/585; 427/578; 427/579; 427/588

(58) **Field of Search** ..... 438/694, 697, 438/784, 787, 788, 911; 427/585, 578, 579, 588

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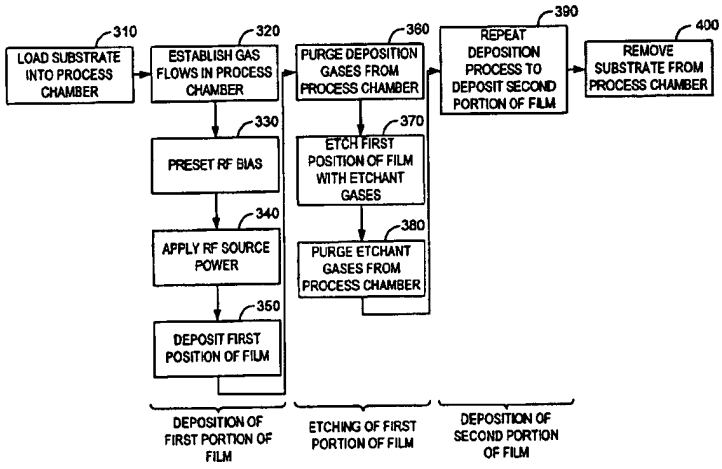
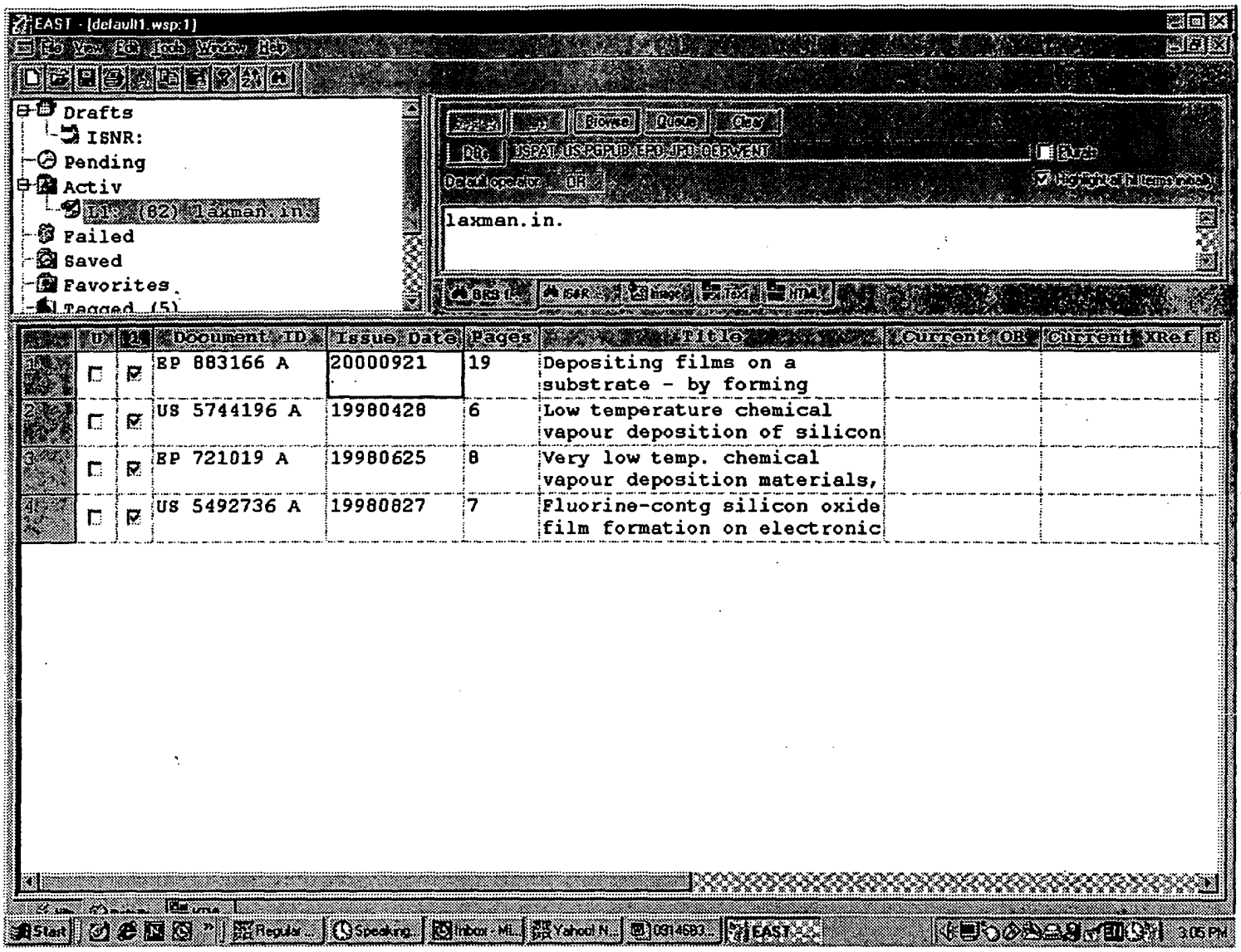
(57) **ABSTRACT**

A method and apparatus are disclosed for depositing a dielectric film in a gap having an aspect ratio at least as large as 6:1. By cycling the gas chemistry of a high-density-plasma chemical-vapor-deposition system between deposition and etching conditions, the gap may be substantially 100% filled. Such filling is achieved by adjusting the flow rates of the precursor gases such that the deposition to sputtering ratio during the deposition phases is within certain predetermined limits.

**15 Claims, 6 Drawing Sheets**

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## Summary

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| US006090682 | 9 | 9 | 0 |
| Total (1) | 9 | 9 | 0 |

(a) applying a fluorinated silicate film onto a substrate;
(b) exposing the fluorinated silicate film to electron beam irradiation under conditions sufficient to stabilize the fluorinated silicate film compared to the fluorinated silicate film prior to such exposure.
(c) imagewise patterning the fluorinated silicate film to form vias in the film extending to the substrate;
(d) optionally patterning the fluorinated silicate layer to form trenches in the film;
(e) depositing a metal into the vias, the optional trenches, and onto a top surface of the fluorinated silicate layer;
(f) removing the metal from the top surface of the fluorinated silicate layer.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a fluorinated silicate film deposited on a substrate.

FIG. 2 shows the fluorinated silicate film being exposed by an electron beam.

FIG. 3 shows a schematic representation of an electron beam modification of fluorinated silicate.

FIG. 4 shows a schematic representation of an electron beam modification of fluorinated silicate in a Damascene process.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As a first step in the process of the invention, a fluorinated silicate such as a fluorinated silicate glass, for example a fluorinated silicon dioxide film is deposited onto a substrate by any means known in the art.

Typical substrates are those suitable to be processed into an integrated circuit or other microelectronic device. Suitable substrates for the present invention non-exclusively include semiconductor materials such as gallium arsenide (GaAs), germanium, lithium niobate, silicon and compositions containing silicon such as silicon germanium, crystalline silicon, polysilicon, amorphous silicon, epitaxial silicon, and silicon dioxide ($SiO_2$) and mixtures thereof

On the surface of the substrate is an optional pattern of raised lines, such as metal, oxide, nitride or oxynitride lines which are formed by well known lithographic techniques. Suitable materials for the lines include silica, silicon nitride, titanium nitride, tantalum nitride, aluminum, aluminum alloys, copper, copper alloys, tantalum, tungsten and silicon oxynitride. These lines form the conductors or insulators of an integrated circuit. Such are typically closely separated from one another at distances of about 20 micrometers or less, preferably 1 micrometer or less, and more preferably from about 0.05 to about 1 micrometer.

The fluorinated silicate film may be applied to the substrate via chemical vapor deposition such as by low pressure chemical vapor deposition LPCVD, plasma-enhanced chemical vapor deposition PECVD, atmospheric pressure chemical vapor deposition APCVD, or subatmospheric chemical vapor deposition SACVD. One method of fluorinated silicon oxide film deposition is taught in U.S. Pat. No. 5,876,798 where films of fluorinated silicon oxide are deposited by means of CVD at reduced pressure using fluorotriethoxysilane (FTES) and tetra-exthyloxysilane (TEOS) as the precursors, together with ozone (mixed with oxygen). A CVD reaction chamber is maintained at a temperature between about 400° C. and 500° C. and at a pressure between about 200 and 260 torr. The thickness of the deposited layer is from about 1,000 to about 20,000 Angstroms.

Other methods of forming films of fluorinated silicon oxide are taught in U.S. Pat. Nos. 5,807,785 and 5,660,895 and 5,492,736. Using, a PECVD process tetraethoxysilane (TEOS) and a fluorine-containing compound may create a layer with a dielectric constant of less than 4.0, preferably approximately 3.5. In a preferred embodiment, the fluorine compounds used are $SiF_4$ or $C_2F_6$. Film deposition may be conducted with a Plasma Therm model VII-70 PECVD system or a Vactronics Model PECVD-2000-M. The plasma enhanced chemical vapor deposition (PECVD) of silicon oxyfluoride films may be carried out using a liquid source and oxygen as a reactive gas. Oxygen and vapors of the source are introduced into the reactor. Source material is introduced at 10–200 sccm and $O_2$ is introduced at between 10 and 200 sccm into the reactor. A heating element is maintained at from about 100° C. to about 600° C., and the total pressure of the reactor is from about 100 mT to about 2 Torr. Plasma power is maintained at from about 50 to about 100 watts of power by a plasma generating system. The deposition rates obtained using these conditions are from about 50 to about 250 angstroms per minute and exhibit an index of refraction of from about 1.377 to about 1.406. These indices of refraction increase with time when exposed to air. Chemical vapor deposition processes are well known to those skilled in the art and chemical vapor deposition reactors are widely commercially available. One suitable reactor is model SK-23-6-93 commercially available from Vactronic Equipment Labs of Bohemia, N.Y.

The film is then treated by exposing it to a flux of electrons. Such a treatment is performed by placing the coated substrate inside the chamber of a large area electron beam exposure system, such as that described in U.S. Pat. No. 5,003,178 to Livesay, the disclosure of which is incorporated herein by reference. This apparatus exposes the entire film to a flood electron beam flux all at once. The period of electron beam exposure will be dependent on the total dosage applied, the electron beam energy applied to the film and the beam current density. One of ordinary skill in the art can readily optimize the conditions of exposure. Preferably the electron beam exposure is done at a vacuum in the range of from about $10^{-5}$ to about $10^{2}$ torr, and with a substrate temperature in the range of from about 20° C. to about 600° C. more preferably from about 100° C. to about 500° C. When the electron beam is used both for fluorine stabilization and surface treatment, energy will fall into the range of from about 0.5 to about 100 KeV, preferably from about 1 to about 20 KeV and more preferably from about 1 to about 8 KeV. The electron beam exposing is preferably conducted from a source which generates an electron beam current of from about 1 to about 150 mA more preferably, from about 1.0 mA to about 30 mA. The electron beam dose will fall into the range of from about 1 to about 500,000 $\mu C/cm^2$, preferably from about 100 to about 10,000 $\mu C/cm^2$, and more preferably from about 100 to about 10,000 $\mu C/cm^2$. The dose and energy selected will be proportional to the thickness of the film to be processed. The appropriate doses and energies may easily be determined by those skilled in the art for the case at hand. Generally the exposure will range from about 0.5 minute to about 120 minutes, and preferably from about 1 minute to about 60 minutes. The film coated substrate may be exposed to electron beams in any chamber having a means for providing electron beam radiation to substrates placed therein. The film is preferably subjected to an electron beam radiation from a uniform large-area electron beam source under conditions sufficient to stabilize the full width and full thickness of the fluorinated silicate film. Preferably the exposure is conducted with an

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is also invoked by the chamber manager subroutine **77***a* and receives a target, or setpoint, temperature parameter. The heater control subroutine **87** measures the temperature by measuring voltage output of a thermocouple located in a susceptor **12**, compares the measured temperature to the setpoint temperature, and increases or decreases current applied to the lamp module **26** to obtain the setpoint temperature. The temperature is obtained from the measured voltage by looking up the corresponding temperature in a stored conversion table, or by calculating the temperature using a fourth order polynomial. When radiant lamps are used to heat the susceptor **12**, the heater control subroutine **87** gradually controls a ramp up/down of current applied to the lamp. The gradual ramp up/down increases the life and reliability of the lamp. Additionally, a built-in fail-safe mode can be included to detect process safety compliance, and can shut down operation of the lamp module **26** if the process chamber **15** is not properly set up.

The above CVD system description is mainly for illustrative purposes and should not necessarily be considered as limiting the scope of the present invention. Additionally, other substrate processing equipment may be employed or variations in the above described system such as variations in susceptor design, heater design, and others are possible. For example, the wafer could be supported and heated by a resistively-heated platen. The dielectric layer and method for forming such a layer of the present invention is not necessarily limited to any specific apparatus.

## II. Exemplary Structure

FIG. **2** illustrates a simplified cross-sectional view of an integrated circuit **200** according to the present invention. As shown, integrated circuit **200** includes NMOS and PMOS transistors **203** and **206**. Each transistor **203** and **206** comprises a source region **212**, a drain region **215** and a gate region **218**. The transistors are separated and electrically isolated from each other by a field oxide region **220**.

A premetal dielectric layer **221** separates transistors **203** and **206** from metal layer **240** with connections between metal layer **240** and the transistors made by contacts **224**. Metal layer **240** is one of four metal layers (**240**, **242**, **244**, and **246**) included in integrated circuit **200**. Each metal layer is separated from adjacent metal layers by respective intermetal dielectric layers **227**, **228**, and **229**. Adjacent metal layers are connected at selected openings by vias **226**. Deposited over metal layer **246** are planarized passivation layers **230**.

While the dielectric layer of the present invention may find uses in each of the dielectric layers shown in integrated circuit **200**, physical properties of the film such as its low dielectric constant and good gap-fill properties make it most useful as an insulation layer between adjacent metal layers, as shown by IMD layers **227**, **228**, and **229**. Typically, such IMD layers are between 0.2 and 0.6 $\mu$m thick. As seen in FIG. **2**, in further processing steps, vias **226** that are formed in the IMD layers also need to be filled adequately. As mentioned above, such IMD layers are often formed of a thick composite insulating layer, such as a thick USG film capped with a PECVD film, in order to manage stress. With such thick composite films used as IMD layers, problems of filling deep vias in the composite insulating layer may be encountered in some applications.

In the present invention, a halogen-doped silicon oxide film, preferably an FSG film, may be formed by a thermal SACVD process and related apparatus. The thickness of the halogen-doped silicon oxide film used for an IMD layer depends on the height of the structures forming the gap to be filled. In typical applications, the deposited halogen-doped silicon oxide film thickness will be sufficient, about 60% of the height of the structures, to fill the gaps. As mentioned above, it is desirable for films used as IMD layers to have an overall low compressive stress. In contrast to thick $O_3$/TEOS USG films that have high tensile stress levels and require thick PECVD capping films to manage the overall intrinsic film stress, halogen-doped silicon oxide films have low compressive intrinsic stress and do not require such thick PECVD capping films to manage overall film stress and prevent film cracking. Instead, a much thinner PECVD capping layer (e.g., 1000 Å thick in some embodiments) may be used in order to produce an IMD layer (made of the FSG film and the thin PECVD capping layer) which has an overall low compressive stress. Of course, a thin PECVD capping layer may be deposited and remain on the FSG film to provide the thin composite film with low compressive stress, or a thick PECVD capping layer may be deposited on the FSG film and subjected to a CMP step to provide the thin composite film with low compressive stress. Because the capped FSG layer of the present invention is relatively thin compared to a thick capped $O_3$/TEOS USG layer, problems of filling deep vias in the composite insulating layer are also minimized.

It should be understood that the simplified integrated circuit **200** is for illustrative purposes only. One of ordinary skill in the art could implement the present method for fabrication of other integrated circuits such as microprocessors, application-specific integrated circuits (ASICs), memory devices, and the like.

## III. Exemplary FSG Film Deposition Using SACVD

An exemplary process for depositing a film of halogen-doped silicon oxide film, such as FSG, which is suitable for use as an IMD layer having low compressive stress and relatively thin film thickness, is discussed below. The SACVD thermal process provides an FSG film having good gap-fill properties and low tensile stress at low temperatures and high deposition rates, according to preferred embodiments of the present invention.

The exemplary process deposits a film of FSG using triethoxyfluorosilane (TEFS) as a source of fluorine at a sub-atmospheric pressure. First, processor **34** controls the motor to load the substrate being processed onto susceptor **12** in vacuum chamber **15** through a vacuum-lock door and to move the substrate into processing position **14**. In processing position **14**, the susceptor and substrate generally are positioned about 200–600 mil from the gas distribution manifold and are preferably positioned about 250 mil from the manifold.

Once the substrate is properly positioned, processor **34** sets and maintains the pressure of the reaction chamber within a range of about 60–650 torr. Preferably, the pressure is maintained within the range of about 200–500 torr, and most preferably it is maintained at about 450 torr. Processor **34** also controls heater **26** to heat the substrate and susceptor to a temperature of between about 200–500° C. Preferably, the substrate and susceptor are heated to a temperature within the range of between about 350–450° C. and most preferably to about 400° C. This temperature range is maintained throughout the deposition.

A process gas is then introduced into the chamber from manifold **11**. The process gas includes reactant gases containing fluorine, silicon, and oxygen. In a preferred

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(74)代理人　弁理士　京本　直樹　(外２名)

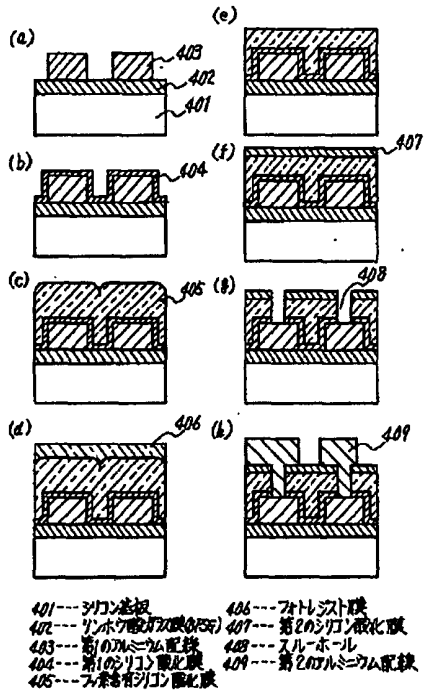
(54)【発明の名称】　半導体装置の製造方法

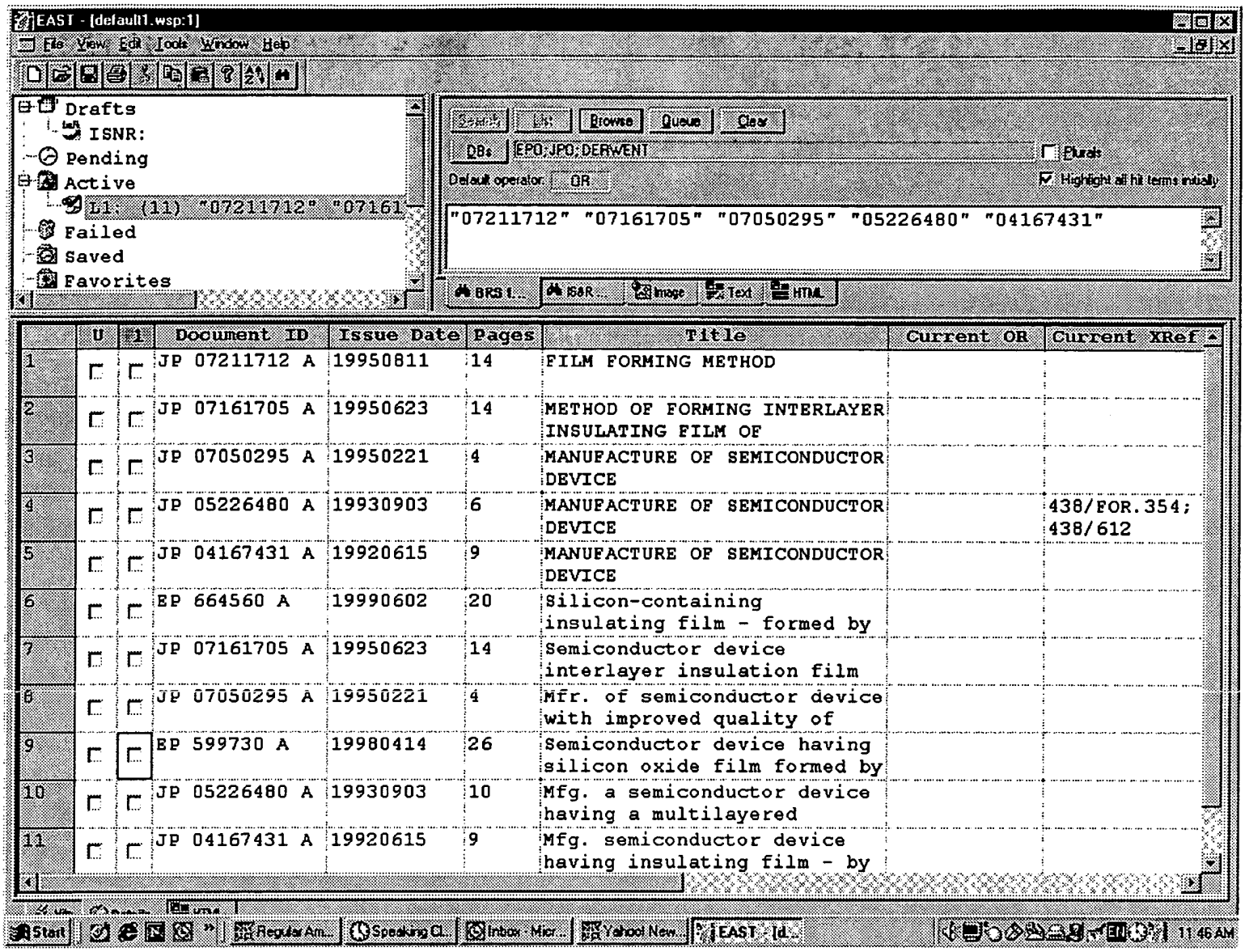
(57)【要約】

【目的】本発明の目的は、多層配線層間絶縁膜の低温（２００℃以下）形成とエッチバック平坦化によって信頼性の優れた多層配線構造体の製造方法を提供することにある。

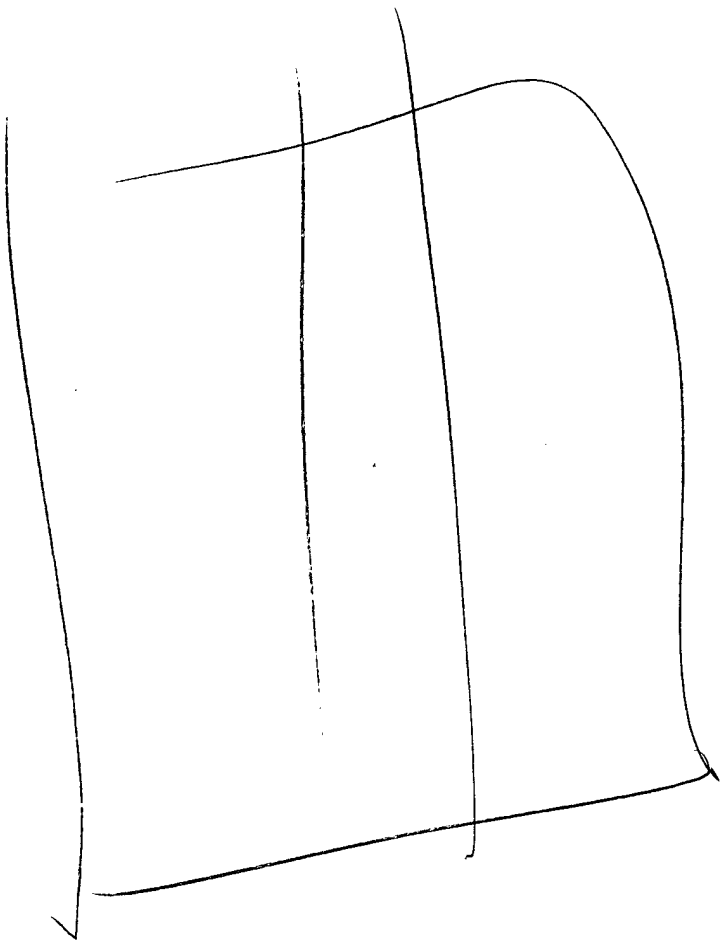
【構成】第１の配線層上に、圧縮圧力を有するシリコン酸化膜を形成した後、フッ素含有シリコン酸化膜を２００℃以下の温度で厚く（２～３．５μｍ）形成した後、フォトレジスト等の平坦化膜を形成しエッチバックによりフッ素含有シリコン酸化膜表面を平坦化する。次に、再び圧縮応力を有するシリコン酸化膜を形成し、所定の位置にスルーホールを形成し、第２の配線層を形成する。

【効果】層間絶縁膜の一部にフッ素含有シリコン酸化膜を用いることにより、耐クラック性，平坦性及び信頼性が向上する。






| | U | #1 | Document ID | Issue Date | Pages | Title | Current OR | Current XRef |
|---|---|---|---|---|---|---|---|---|
| 1 | ☐ | ☐ | JP 07211712 A | 19950811 | 14 | FILM FORMING METHOD | | |
| 2 | ☐ | ☐ | JP 07161705 A | 19950623 | 14 | METHOD OF FORMING INTERLAYER INSULATING FILM OF | | |
| 3 | ☐ | ☐ | JP 07050295 A | 19950221 | 4 | MANUFACTURE OF SEMICONDUCTOR DEVICE | | |
| 4 | ☐ | ☐ | JP 05226480 A | 19930903 | 6 | MANUFACTURE OF SEMICONDUCTOR DEVICE | | 438/FOR.354; 438/612 |
| 5 | ☐ | ☐ | JP 04167431 A | 19920615 | 9 | MANUFACTURE OF SEMICONDUCTOR DEVICE | | |
| 6 | ☐ | ☐ | EP 664560 A | 19990602 | 20 | Silicon-containing insulating film - formed by | | |
| 7 | ☐ | ☐ | JP 07161705 A | 19950623 | 14 | Semiconductor device interlayer insulation film | | |
| 8 | ☐ | ☐ | JP 07050295 A | 19950221 | 4 | Mfr. of semiconductor device with improved quality of | | |
| 9 | ☐ | ☐ | EP 599730 A | 19980414 | 26 | Semiconductor device having silicon oxide film formed by | | |
| 10 | ☐ | ☐ | JP 05226480 A | 19930903 | 10 | Mfg. a semiconductor device having a multilayered | | |
| 11 | ☐ | ☐ | JP 04167431 A | 19920615 | 9 | Mfg. semiconductor device having insulating film - by | | |



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## Document Listing

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|---|---|---|
| US005850105 | 9 | 1 - 9 |
| US005817572 | 27 | 1 - 27 |
| US005792705 | 8 | 1 - 8 |
| US005641712 | 6 | 1 - 6 |
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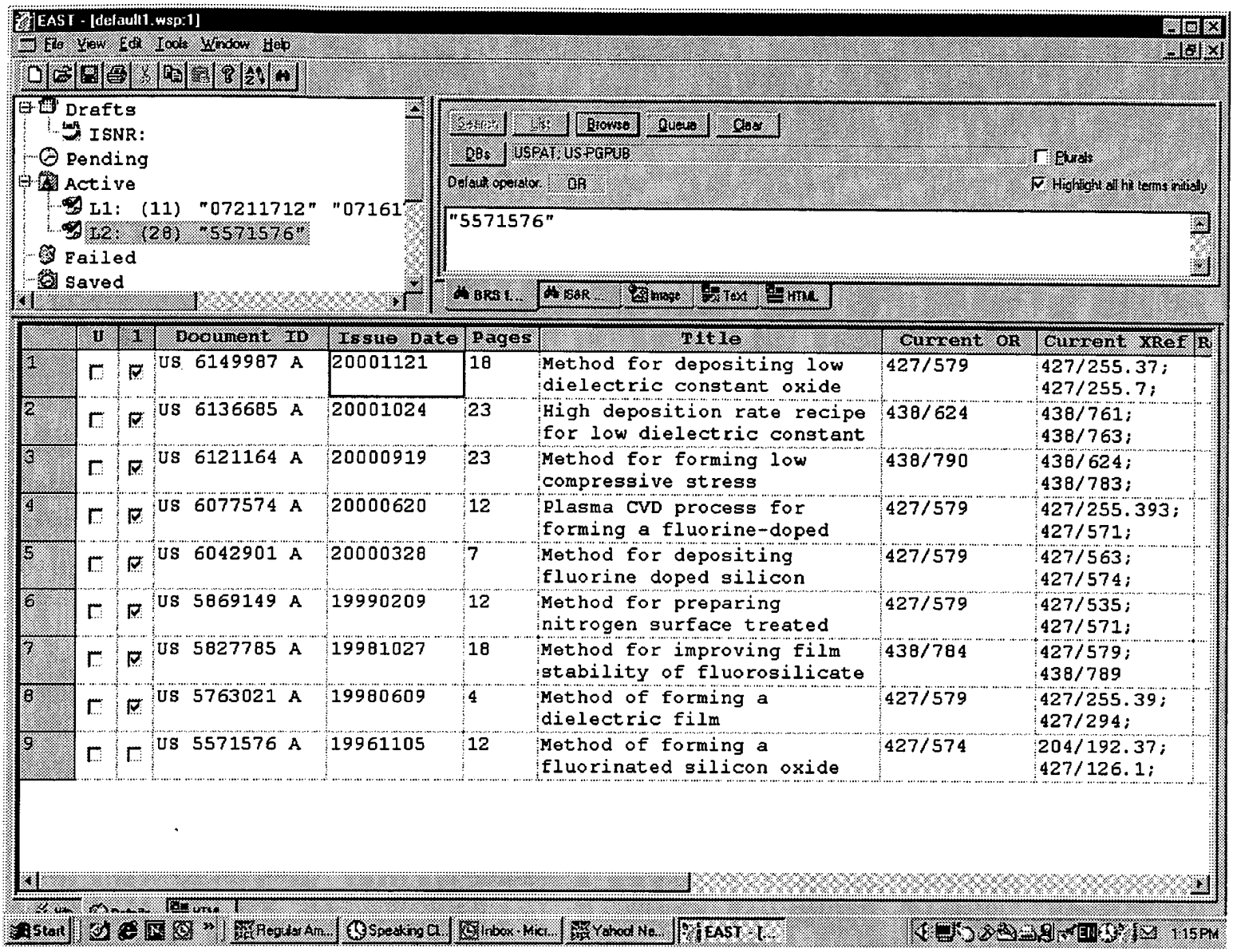


| | U | I | Document ID | Issue Date | Pages | Title | Current OR | Current XRef | R |
|---|---|---|---|---|---|---|---|---|---|
| 1 | ☐ | ☑ | US 6149987 A | 20001121 | 18 | Method for depositing low dielectric constant oxide | 427/579 | 427/255.37; 427/255.7; | |
| 2 | ☐ | ☑ | US 6136685 A | 20001024 | 23 | High deposition rate recipe for low dielectric constant | 438/624 | 438/761; 438/763; | |
| 3 | ☐ | ☑ | US 6121164 A | 20000919 | 23 | Method for forming low compressive stress | 438/790 | 438/624; 438/783; | |
| 4 | ☐ | ☑ | US 6077574 A | 20000620 | 12 | Plasma CVD process for forming a fluorine-doped | 427/579 | 427/255.393; 427/571; | |
| 5 | ☐ | ☑ | US 6042901 A | 20000328 | 7 | Method for depositing fluorine doped silicon | 427/579 | 427/563; 427/574; | |
| 6 | ☐ | ☑ | US 5869149 A | 19990209 | 12 | Method for preparing nitrogen surface treated | 427/579 | 427/535; 427/571; | |
| 7 | ☐ | ☑ | US 5827785 A | 19981027 | 18 | Method for improving film stability of fluorosilicate | 438/784 | 427/579; 438/789 | |
| 8 | ☐ | ☑ | US 5763021 A | 19980609 | 4 | Method of forming a dielectric film | 427/579 | 427/255.39; 427/294; | |
| 9 | ☐ | ☐ | US 5571576 A | 19961105 | 12 | Method of forming a fluorinated silicon oxide | 427/574 | 204/192.37; 427/126.1; | |

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| US006340629 | 6 | 6 | 0 |
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14 pages

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平7－161705

(43)公開日　平成７年(1995)６月23日

| (51)Int.Cl.[6] | 識別記号 | 庁内整理番号 | ＦＩ | 技術表示箇所 |
|---|---|---|---|---|
| Ｈ０１Ｌ 21/316 | | Ｍ 7352－4Ｍ | | |
| 21/768 | | | | |
| | | | Ｈ０１Ｌ 21/ 90 | Ｋ |
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審査請求　有　請求項の数７　ＯＬ　（全 14 頁）

(21)出願番号　特願平5－304196

(22)出願日　平成５年(1993)12月３日

特許法第30条第１項適用申請有り　1993年６月８日、発行の「1993 PROCEED INGS TENTH INTERNATIONAL VLSI MULTIL EVEL INTERCONNECTION CONF ERENCE」に発表

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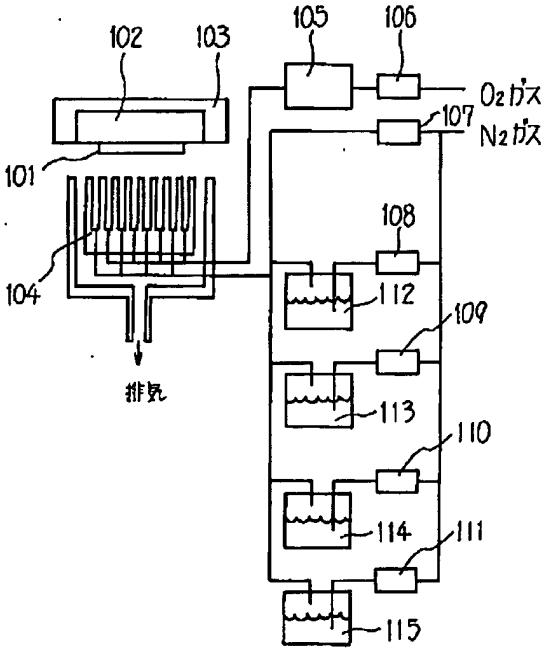
(74)代理人　弁理士　京本　直樹　（外２名）

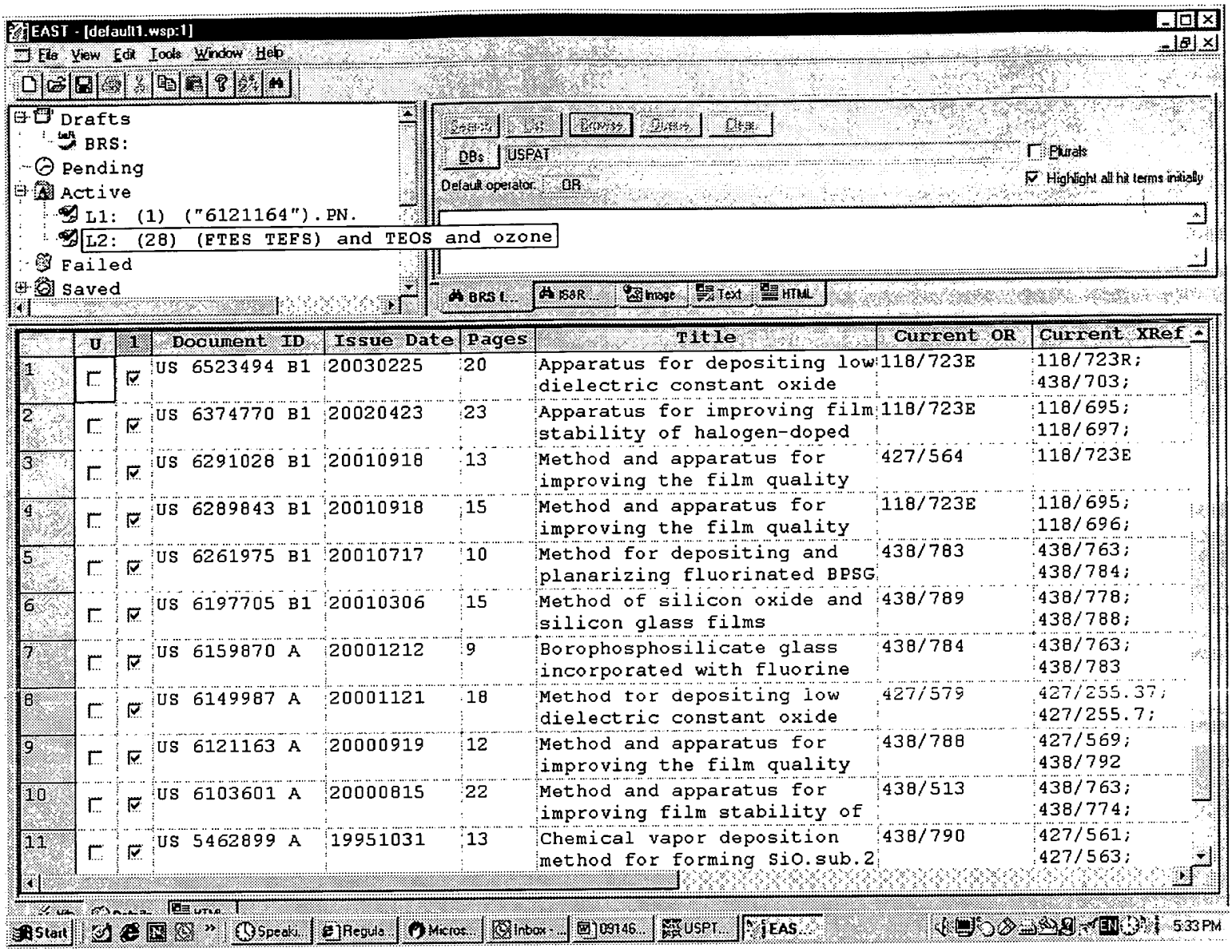
(54)【発明の名称】　半導体装置の多層配線層間絶縁膜の形成方法

(57)【要約】

【目的】微細配線間隙に空洞が発生せず、平坦性に優れ、かつ、残留水分量・吸湿量の少ない多層配線層間絶縁膜の形成方法を提供する。

【構成】炭素数３以上のアルキル基を有するフルオロアルコキシシランをと酸化性ガスとを用いる化学気相成長法を用いてフロー性の高いフッ素含有シリコン酸化膜４０５を形成し、層間絶縁膜の１部に用いる。また、炭素数１以上のアルキル基を有するフルオロアルコキシシランと酸化性ガスとを用いる化学気相成長法において、沸点が９０℃以上の高沸点溶剤を添加せしめることによってフロー性の高いフッ素含有シリコン酸化膜４０５を形成し、層間絶縁膜の１部に用いる。



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| 1 | ☐ | ☑ | US 6523494 B1 | 20030225 | 20 | Apparatus for depositing low dielectric constant oxide | 118/723E | 118/723R; 438/703; |
| 2 | ☐ | ☑ | US 6374770 B1 | 20020423 | 23 | Apparatus for improving film stability of halogen-doped | 118/723E | 118/695; 118/697; |
| 3 | ☐ | ☑ | US 6291028 B1 | 20010918 | 13 | Method and apparatus for improving the film quality | 427/564 | 118/723E |
| 4 | ☐ | ☑ | US 6289843 B1 | 20010918 | 15 | Method and apparatus for improving the film quality | 118/723E | 118/695; 118/696; |
| 5 | ☐ | ☑ | US 6261975 B1 | 20010717 | 10 | Method for depositing and planarizing fluorinated BPSG | 438/783 | 438/763; 438/784; |
| 6 | ☐ | ☑ | US 6197705 B1 | 20010306 | 15 | Method of silicon oxide and silicon glass films | 438/789 | 438/778; 438/788; |
| 7 | ☐ | ☑ | US 6159870 A | 20001212 | 9 | Borophosphosilicate glass incorporated with fluorine | 438/784 | 438/763; 438/783 |
| 8 | ☐ | ☑ | US 6149987 A | 20001121 | 18 | Method for depositing low dielectric constant oxide | 427/579 | 427/255.37; 427/255.7; |
| 9 | ☐ | ☑ | US 6121163 A | 20000919 | 12 | Method and apparatus for improving the film quality | 438/788 | 427/569; 438/792 |
| 10 | ☐ | ☑ | US 6103601 A | 20000815 | 22 | Method and apparatus for improving film stability of | 438/513 | 438/763; 438/774; |
| 11 | ☐ | ☑ | US 5462899 A | 19951031 | 13 | Chemical vapor deposition method for forming SiO.sub.2 | 438/790 | 427/561; 427/563; |

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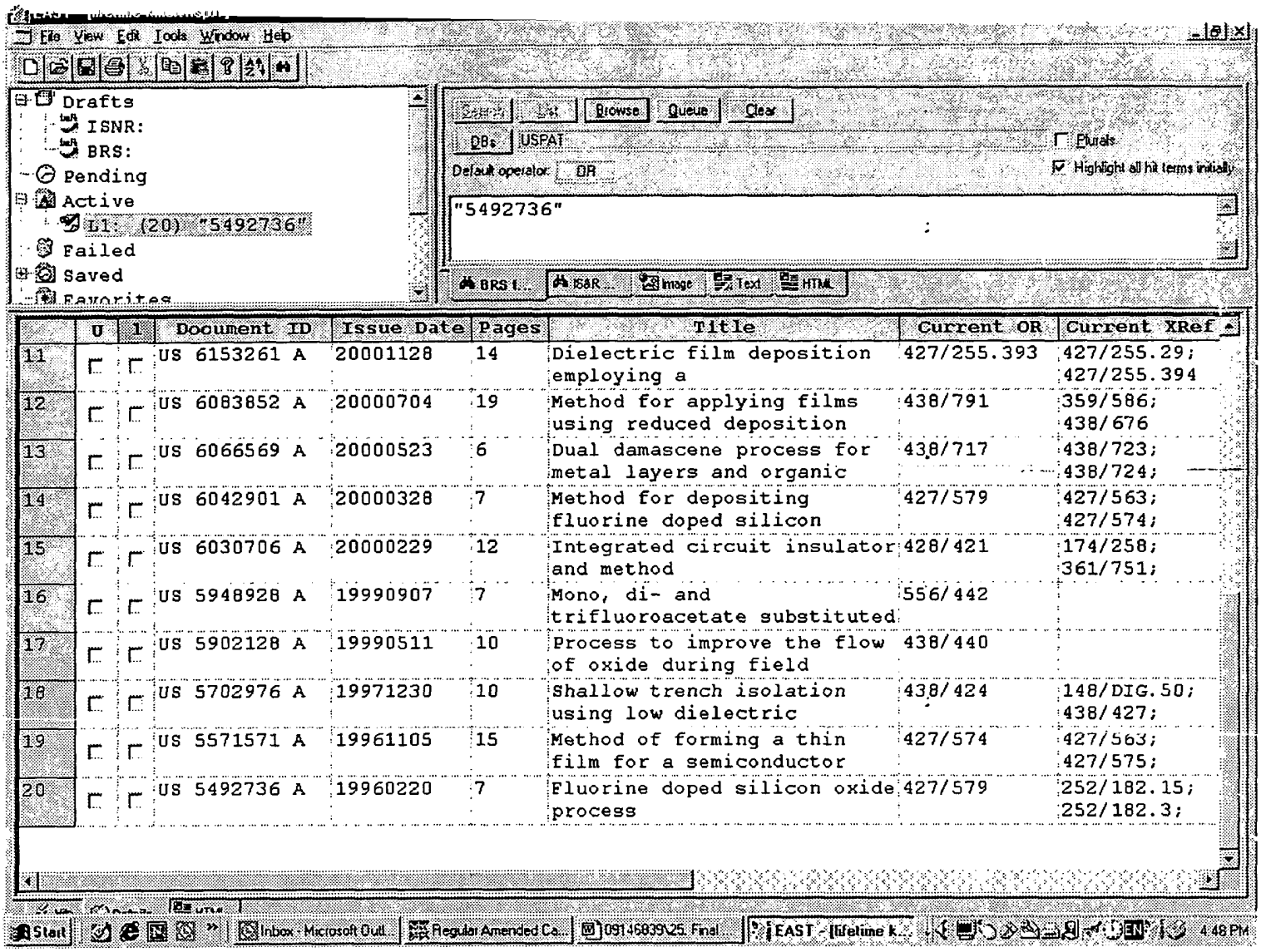
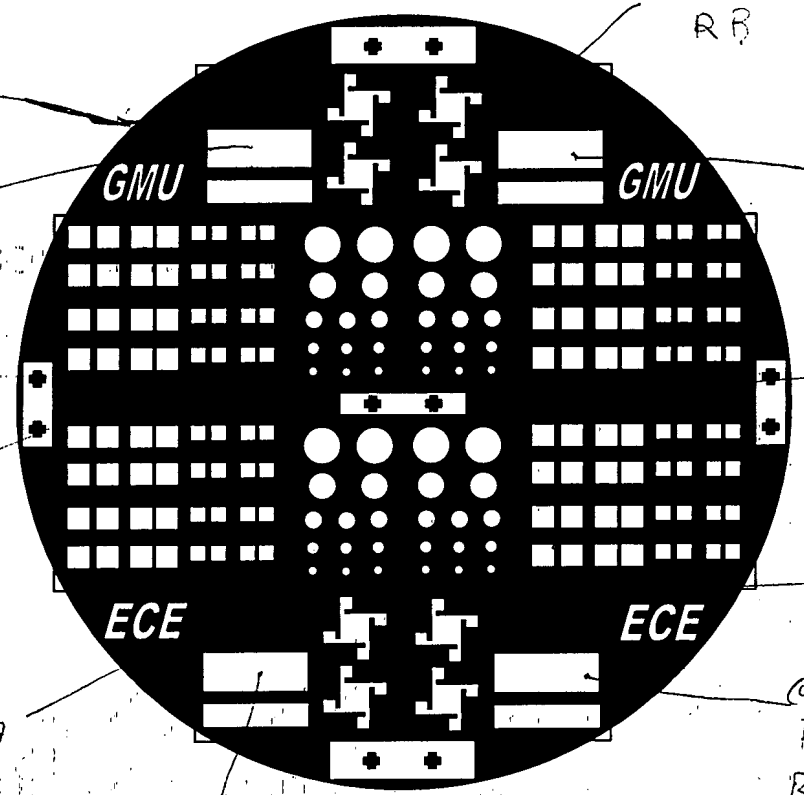



| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR | Current XRef |
|---|---|---|---|---|---|---|---|---|
| 11 | ☐ | ☐ | US 6153261 A | 20001128 | 14 | Dielectric film deposition employing a | 427/255.393 | 427/255.29; 427/255.394 |
| 12 | ☐ | ☐ | US 6083852 A | 20000704 | 19 | Method for applying films using reduced deposition | 438/791 | 359/586; 438/676 |
| 13 | ☐ | ☐ | US 6066569 A | 20000523 | 6 | Dual damascene process for metal layers and organic | 438/717 | 438/723; 438/724; |
| 14 | ☐ | ☐ | US 6042901 A | 20000328 | 7 | Method for depositing fluorine doped silicon | 427/579 | 427/563; 427/574; |
| 15 | ☐ | ☐ | US 6030706 A | 20000229 | 12 | Integrated circuit insulator and method | 428/421 | 174/258; 361/751; |
| 16 | ☐ | ☐ | US 5948928 A | 19990907 | 7 | Mono, di- and trifluoroacetate substituted | 556/442 | |
| 17 | ☐ | ☐ | US 5902128 A | 19990511 | 10 | Process to improve the flow of oxide during field | 438/440 | |
| 18 | ☐ | ☐ | US 5702976 A | 19971230 | 10 | Shallow trench isolation using low dielectric | 438/424 | 148/DIG.50; 438/427; |
| 19 | ☐ | ☐ | US 5571571 A | 19961105 | 15 | Method of forming a thin film for a semiconductor | 427/574 | 427/563; 427/575; |
| 20 | ☐ | ☐ | US 5492736 A | 19960220 | 7 | Fluorine doped silicon oxide process | 427/579 | 252/182.15; 252/182.3; |

MA1 2/24/01

Level 1: Starting wafer is lightly doped p-type Si 4-inch wafer. There is an oxide layer which has already been grown (approximately 5000 Angstroms). This photoresist mask will be used to pattern the oxide by dipping in an oxide etchant. The oxide remaining will be used as the dopant mask for the $n^+$ spin-on doping process.




@100 μA
FB=130
RB=126

@4000 μA
FB=5.8
RB=5.8

@100 μA
FB=73.6
RB=75.3

@100 μA
FB=70
RB=68.5

@4000 μA
FB=5.4
RB=5.4

@100 μA
FB=28.5
RB=22.2

@4000 μA
F.B=5.3
R.B=5.3

@100 μA
F.B=63.7
R.B=57.8

@100 μA
F.B=3.6
R.B=3.1

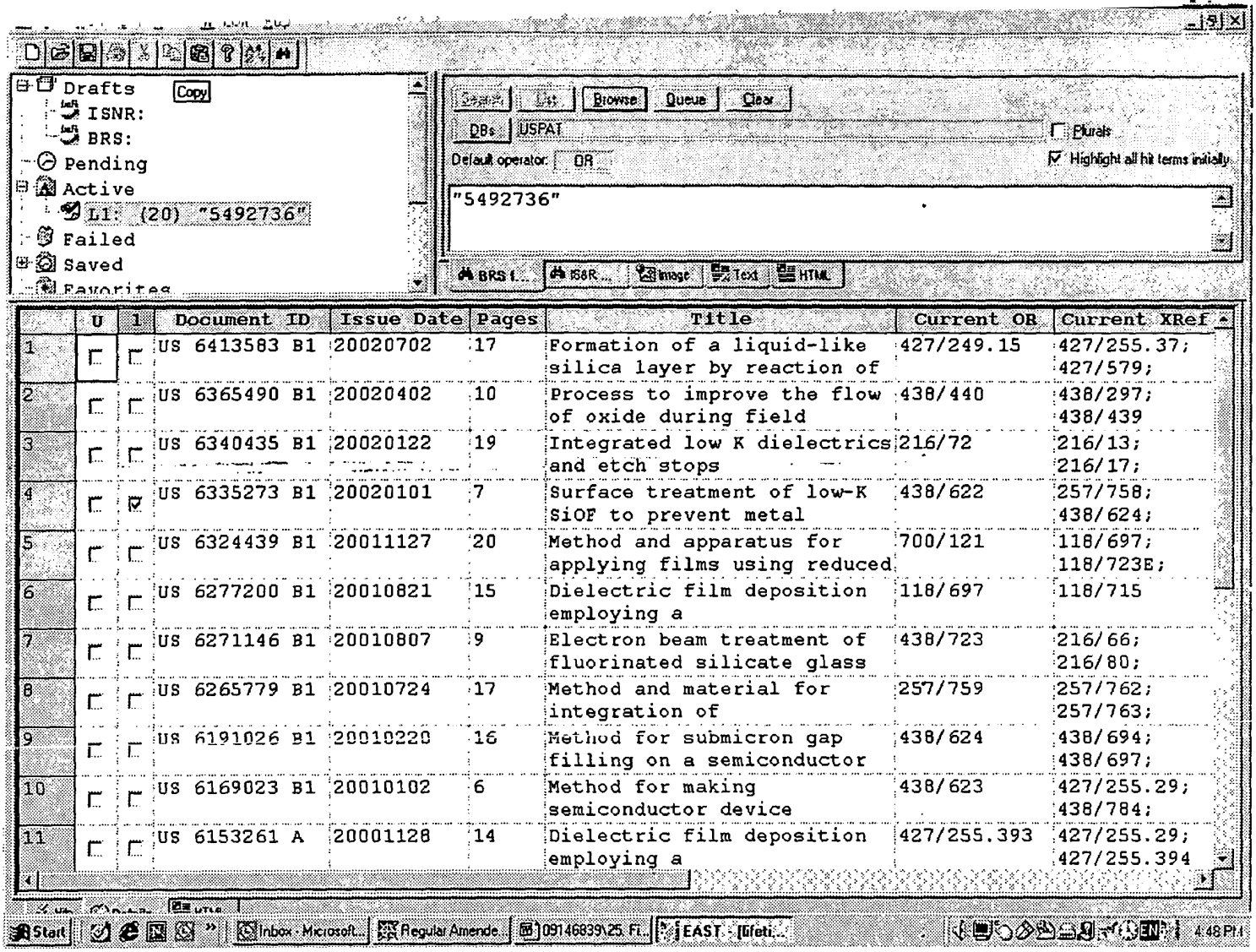
@4000 μA
F.B=8.5
R.B=8.7

Level 1: n+ doping

BACKSIDE:

FB - 33.6, 31.8

RB - 33.5, 31.4




| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR | Current XRef |
|---|---|---|---|---|---|---|---|---|
| 1 | ☐ | ☐ | US 6413583 B1 | 20020702 | 17 | Formation of a liquid-like silica layer by reaction of | 427/249.15 | 427/255.37; 427/579; |
| 2 | ☐ | ☐ | US 6365490 B1 | 20020402 | 10 | Process to improve the flow of oxide during field | 438/440 | 438/297; 438/439 |
| 3 | ☐ | ☐ | US 6340435 B1 | 20020122 | 19 | Integrated low K dielectrics and etch stops | 216/72 | 216/13; 216/17; |
| 4 | ☐ | ☑ | US 6335273 B1 | 20020101 | 7 | Surface treatment of low-K SiOF to prevent metal | 438/622 | 257/758; 438/624; |
| 5 | ☐ | ☐ | US 6324439 B1 | 20011127 | 20 | Method and apparatus for applying films using reduced | 700/121 | 118/697; 118/723E; |
| 6 | ☐ | ☐ | US 6277200 B1 | 20010821 | 15 | Dielectric film deposition employing a | 118/697 | 118/715 |
| 7 | ☐ | ☐ | US 6271146 B1 | 20010807 | 9 | Electron beam treatment of fluorinated silicate glass | 438/723 | 216/66; 216/80; |
| 8 | ☐ | ☐ | US 6265779 B1 | 20010724 | 17 | Method and material for integration of | 257/759 | 257/762; 257/763; |
| 9 | ☐ | ☐ | US 6191026 B1 | 20010220 | 16 | Method for submicron gap filling on a semiconductor | 438/624 | 438/694; 438/697; |
| 10 | ☐ | ☐ | US 6169023 B1 | 20010102 | 6 | Method for making semiconductor device | 438/623 | 427/255.29; 438/784; |
| 11 | ☐ | ☐ | US 6153261 A | 20001128 | 14 | Dielectric film deposition employing a | 427/255.393 | 427/255.29; 427/255.394 |

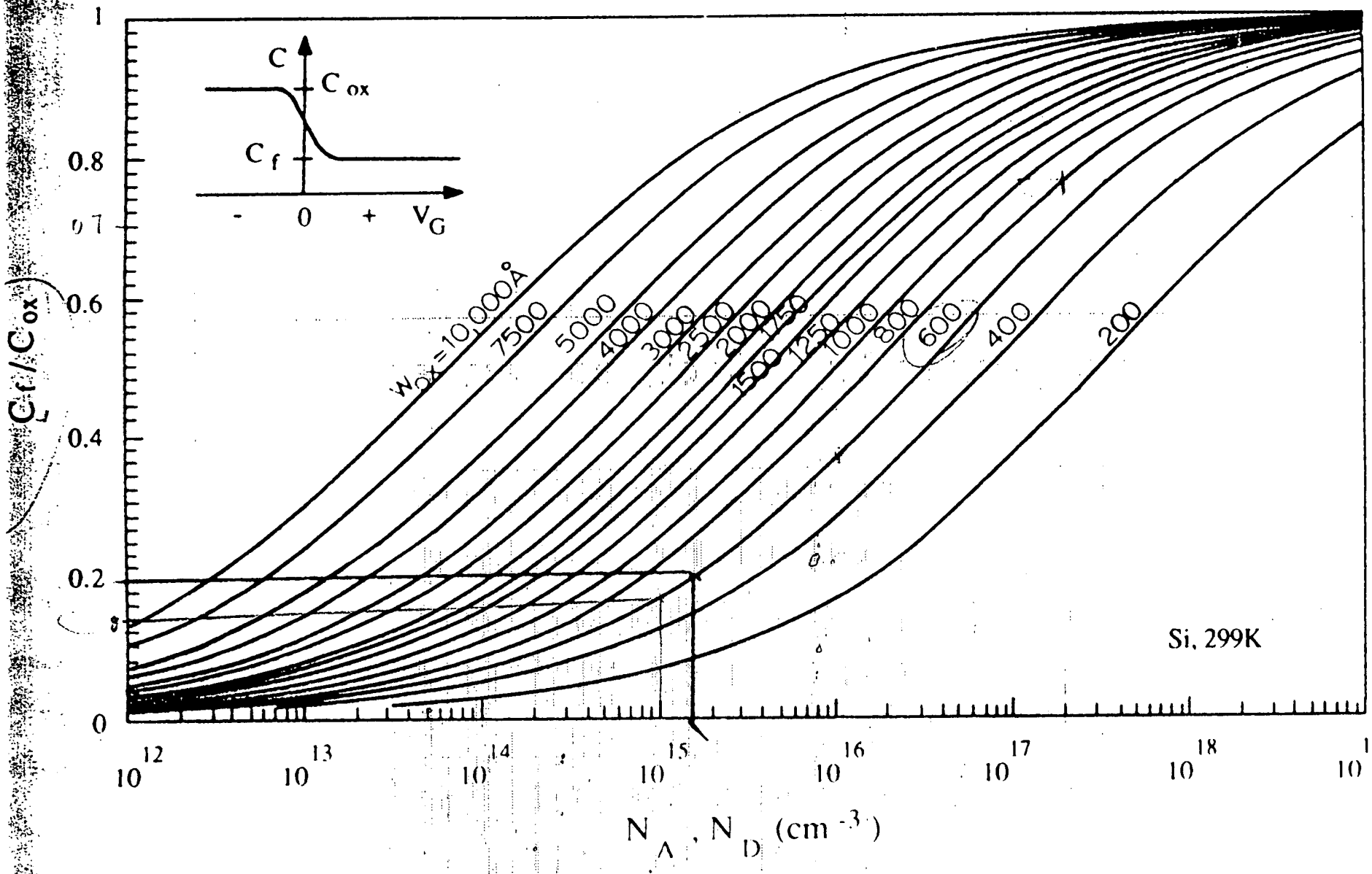



**Fig. 2.7** Curves of $C_f/C_{ox}$ versus doping concentration as a function of oxide thickness for silicon at $T = 300$ K.